2827

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicants:	Christopher J. Kelly, et al.	§	Art Unit:	2827
Serial No.:	09/955,230	§	Examiner:	Tuan T. Dinh
Filed:	September 18, 2001	§		
Title:	Printed Circuit Board Routing and Power Delivery for High Frequency Integrated Circuits	§	Docket No.	ITL.0644US (P12307)

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

REPLY TO OFFICE ACTION DATED JUNE 3, 2003

Dear Sir:

In an Office Action mailed on June 3, 2003, claims 1-29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Selna in view of Jones. These rejections are addressed below.

Rejections of Claims 1-14:

The printed circuit board of independent claim 1 includes a signal layer and a supply voltage plane that is embedded in the signal layer to supply power to multiple supply voltage pins of a component that is mounted to the printed circuit board.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 1 for at least the reason that neither cited reference teaches or suggests a supply voltage plane that is embedded in a signal layer. More specifically, the Examiner labels the Vss trace 8C as

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I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

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allegedly being the supply voltage plane of claim 1. However, contrary to the Examiner's position, Selna teaches that the Vss plane 60 is the supply voltage plane, not the Vss trace 8C that communicates power from the Vss plane 60 to the mounted component. As depicted in Fig. 2 of Selna, the Vss plane 60 is located below the signal layer that contains the trace 8C and is therefore not embedded in the signal layer. Thus, Selna neither teaches nor suggests a supply voltage plane that is embedded in signal layer. Furthermore, Jones does not teach or suggest the missing claim limitations. Therefore, even assuming, for purposes of argument, that the combination of Jones and Selna is proper, this combination does not teach or suggest all claim limitations; and for at least this reason, a *prima facie* case of obviousness has not been set forth for independent claim 1.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 1 for at least the additional, independent reason that the Examiner does not point out where the prior art contains the alleged suggestion or motivation to combine Selna and Jones. More specifically, the Examiner must show, with specific citations to the prior art, where the prior art contains support for the alleged suggestion or motivation for the combination. *Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143. Therefore, for at least this additional, independent reason, a *prima facie* case of obviousness has not been established for independent claim 1.

Claims 2-14 are patentable for at least the reason that these claims depend from an allowable claim.

Rejections of Claims 15-19:

The printed circuit board of claim 15 includes a supply voltage plane layer and a ground plane that is embedded in the supply voltage plane layer to provide ground connections to multiple pins of a component that is mounted to the printed circuit board.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 15 for at least the reason that the combination of Jones and Selna fails to teach or suggest all claim limitations. For example, the Examiner relies on Selna to allegedly teach a ground plane that is embedded in a supply voltage plane layer. The Examiner labels the Vss plane 60 as the

alleged supply voltage plane layer. However, the Examiner fails to point and Applicant cannot find where Selna allegedly discloses a ground plane that is embedded in the Vss plane 60. Furthermore, Jones fails to teach or suggest the missing claim limitations. Thus, for at least the reason that the combination of Selna and Jones fails to teach or suggest all claim limitations, a *prima facie* case of obviousness has not been established for independent claim 15.

The Examiner fails to establish a *prima facie* case of obviousness for independent claim 15 for at least the additional, independent reason that the Examiner fails to specifically show where the prior art contains the alleged suggestion or motivation to combine Selna and Jones. See discussion of this point in the discussion of the rejection of claim 1 above.

Claims 16-19 are patentable for at least the reason that these claims depend from an allowable claim.

Rejections of Claims 20-26:

The method of independent claim 20 recites for each high frequency component to be mounted on a printed circuit board, embedding an associated supply voltage plane in a signal layer of the printed board.

See discussion of claim 1 above. In particular, neither Jones nor Selna allegedly teaches a supply voltage plane that is embedded in a signal layer, and for at least this reason, a *prima facie* case of obviousness has not been established for independent claim 20. Furthermore, the Examiner fails to specifically show where the prior art contains the alleged suggestion or motivation for the combination of Jones and Selna, and for at least this additional, independent reason, fails to establish a *prima facie* case of obviousness for independent claim 20.

Claims 21-26 are patentable for at least the reason that these claims depend from an allowable claim.

Rejections of Claims 27-29:

The method of claim 27 recites for each high frequency component to be mounted on a printed circuit board, embedding an associated ground plane in a supply voltage plane layer of the printed circuit board.

See discussion of claim 15 above. In particular, the Examiner fails to establish a *prima facie* case of obviousness for independent claim 27 for at least the reason that neither Selna nor Jones teaches or suggests embedding a ground plane in a supply voltage plane layer. Additionally, the Examiner fails to establish a *prima facie* case of obviousness for independent claim 27 for at least the additional, independent reason that the Examiner fails to specifically show where the prior art contains the alleged suggestion or motivation to combine Selna and Jones.

Claims 28 and 29 are patentable for at least the reason that these claims depend from an allowable claim.

CONCLUSION

In view of the foregoing, withdrawal of the §103 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0644US).

Respectfully submitted,

Date: June 13, 2003

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